IN THE SPECIFICATION

At page 6 of the specification, at line 30, please replace the following paragraph:

Figure 5, comprising Figures 5A and 5B, illustrates further details of a logic bank, a horizontal breaker, and a vertical breaker.

At page 7 of the specification, at line 1, please replace the following paragraph:

Figure 6, comprising Figures 6A, 6B, and 6C, shows a vertical breaker tile including multi-purpose buses.

At page 14 of the specification, at line 21, please replace the following paragraph:

CPU 206 also controls the selective enabling of PIOs 201A in step 325, thereby providing certain output signals before other output signals from CSoC 101. A more detailed description of PIOs 201A is provided in U.S. Patent Application No. 09/418,416, filed on October 15, 1999 (now U.S. Patent No. 6,624,656 B1) by Triscend Corporation, and entitled "An Input/Output Circuit With User Programmable Functions."

At page 17 of the specification, at line 1, please replace the following paragraph:

Specifically referring to Figure 5, which comprises Figures 5A and 5B, from each corner breaker 404, the address signals sw_adr[31:0] are distributed to the horizontal breaker 403 immediately below the corner breaker 404. These address signals are then distributed to the logic bank 401 to the right of horizontal breaker 403. Selection of the configuration memory cells within each logic block tile 501 is performed using well known circuitry and methods and therefore is not discussed in detail herein.

At page 17 of the specification, at line 25, please replace the following paragraph:

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In accordance with the present invention, the buses for distributing the write data and read data signals can be used for both configuration memory and user data, thereby providing an extremely efficient and flexible resource on CSoC 101. Figure 6, which comprises Figures 6A, 6B, and 6C, illustrates one embodiment of a vertical breaker tile 502 including such dual-purpose buses. Specifically, bus 601 distributes the write data signals sw_dws. Registers 602 provide a registered version of those signals (fw_dws) to the configuration memory cells in the appropriate logic block tiles 501. In this embodiment, the same data is provided to every logic block tile 501 in the column of tiles, thereby providing flexibility in the placement of resources connected to bus 601. Row select circuitry, well known to those skilled in the art, is used to determine which of those logic block tiles 501 should receive the configuration data.

At page 18 of the specification, at line 31, please replace the following paragraph:

Determining the states of the configuration memory cells in logic block tiles 501 is highly advantageous in debug operations. For a more detailed description of such debug operations, see U.S. Patent Application No. 09/418,948, entitled "Bus Mastering Debugging System For Integrated Circuits", filed by Triscend Corporation on October 15, 1999, now U.S. Patent No. 6,691,266 B1.

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